

Keyboard Encoder

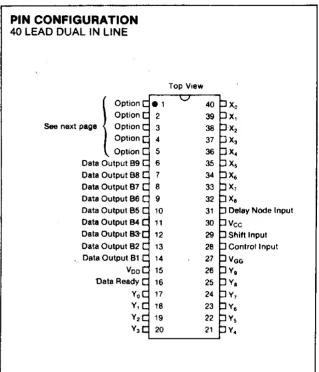
FEATURES

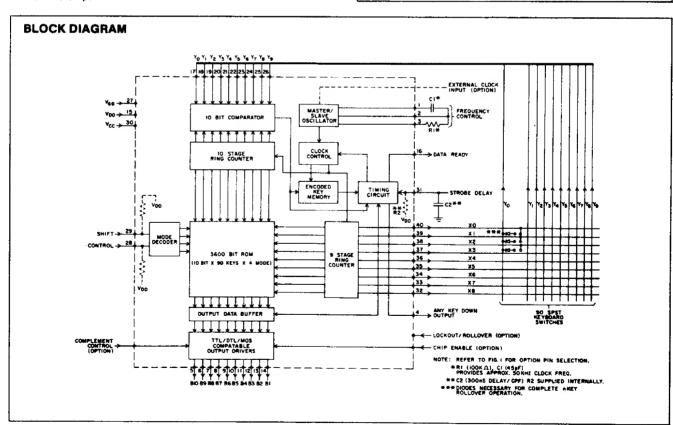
- One integrated circuit required for complete keyboard assembly
- N key rollover or lock out operation
- Quad mode operation
- Lock out/rollover selection under external control (option)
- Self-contained or slave oscillator circuit
- 10 output data bits available
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- Output data buffer register included
- Output enable provided (option)
- External data complement control provided (option)
- Pulse or level data ready output signal provided (option)
- "Any Key Down" output provided (option)
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Programmable coding with a single mask change
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

DESCRIPTION

The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components.

The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.





CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a

substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock

—requires one package pin to input an external clock source. Internal Oscillator

—requires three package pins interconnected with an external RC network to develop the clock required.

Lockout/Rollover (LO/RO)

—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.

Complement Control (CC)

-requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.

Chip Enable (CE)

—requires one package pin to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.

Any Key Output (AKO)

-requires one package pin to indicate a key depression.

Output Data Bit 10 (B10)

---requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:

External Clock + 4 of the following functions

OR

Internal Oscillator + 2 of the following functions LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO LO/RO	CC	CE CE	AKO BIO
External Clock External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	cc	CE	AKO	BIO
			LO/RO	CC
	Internal Oscillator			CE
				AKO
				BIO
				CE
				AKO
			l cc	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC})	20V to +0.3V
Logic input voltages (with respect to Vcc)	20V to +0.3V
Storage Temperature	-65°C to +150°C
Operating Temperature Range	. 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

 $V_{CC} = +5 \text{ Volts } \pm 0.5 \text{ Volts}$

 $V_{GG} = -12 \; \text{Volts} \; \pm 1.0 \; \text{Volts}, \; V_{DD} = GND$

 $(V_{CC} = Substrate Voltage)$

Operating Temperature (T_A)= 0°C to +70°C



ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Тур**	Max	Units	Conditions
Clock Frequency	f	10	50	100	kHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	_	_	μs	i i i i i i i i i i i i i i i i i i i
Clock Input	Vio	1	1	۱	V	
•	VII	V _{cc} -1.4	_	.15 V _{CC} +0.3	ĺv	
Data Input (Shift, Control, Complement Control, Lockout/Rollover, Chip Enable		VGC 1.4		V ₀ C +0.3	*	
& External Clock)			Į.			
Logic "0" Level	Vio	Vaa	l —	+0.75	V	
Logic "1" Level	VI1	V _{cc} -1.1	_	Vcc+0.3	V	
Shift & Control Input	<u> </u>	1	ł	1		
Current	INSC	75	95	120	μΑ	V ₁ = +5V
X Output (X ₀ -X ₈)						ļ
Logic "1" Output Current	Ixi	40	170	400	μA	V _{OUT} = V _{CC} (See Note 2)
		600	1300	2500	μA	$V_{OUT} = V_{CC} - 1.3V$
		900	1600	3500	μA	$V_{OUT} = V_{CC} - 2.0V$
		1500	3800	6000	μA	$V_{OUT} = V_{CC} - 5V$
		3000	6000	10000	μΑ	$V_{OUT} = V_{CC} - 10V$
Logic "0" Output Current	1 _{x0}	8	15	50	μ A	$V_{OUT} = V_{CC}$
		6	11	35	μA	$V_{OUT} = V_{CC} - 1.3V$
		5	10	30	μA	$V_{OU1} = V_{CC} - 2.0V$
	1	2	5	15	μA	$V_{OUT} = V_{CC} - 5V$
		-	0.5	5	μA	$V_{OUT} = V_{CC} - 10V$
Y input (Y ₀ -Y ₉)	1		ł		,	
Trip Level	l V _Y	V _{cc} -5	V _{cc} –3	V _{cc} -2	ν	Y Input Going Positive (See Note
Hysteresis	ΔV_{Y}	0.5	0.9	1.4	v	(See Note 1)
Selected Y Input Current	lys	18	36	100	μA	$V_{IN} = V_{CC}$
	1	14	28	90	μA	$V_{IN} = V_{CC} - 1.3V$
		13	25	80	μΑ	$V_{IN} = V_{CC} - 2.0V$
		6	12	60	μA	$V_{IN} = V_{CC} - 5V$
		_	1	30	μA	$V_{IN} = V_{CC} - 10V$
Unselected Y Input Current	I _{YU}	9	18	50	μΑ	$V_{IN} = V_{CC}$
	1	7	14	45	μΑ	$V_{IN} = V_{CC} - 1.3V$
	ł	6	13	40	μΑ	$V_{IN} = V_{CC} + 2.0V$
	1	3	6	30	μA	$V_{IN} = V_{CC} - 5V$
	ľ	_	0.5	15	μΑ	$V_{IN} = V_{CC} - 10V$
nput Capacitance	CIN	_	3	10	pF	at 0V (All Inputs)
K-Y Precharge			ŭ	'	ן "י	at ov (All Inputs)
Characteristics	φP	1500	3500	5000		
	Ψ'	200	600	5000 1500	μΑ	$V = V_{cc}$
witch Characteristics		200	000	1300	μΑ	$V = V_{cc} - 5$ (See Note 2)
Minimum Switch Closure						.
Contact Closure	-	_		- 1	_	See Timing Diagram
Resistance	Zcc			200	_	
***************************************	Zco	1 × 10 ⁷	_	300	Ω	
Strobe Delay	200	1 ^ 10	_	_	Ω	
Trip Level (Pin 31)	1 . 1			1		
Hysteresis	V _{SD}	V _{cc} -4	V _{cc} −3	V _{cc} -2	V	
Quiescent Voltage (Pin 31)	V _{SD}	0.5	0.9	1.4	V	(See Note 1)
• , ,		-3	-5	-9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	_	_ [_	.55	v	I. — 25m A
	_	_	_	0.8	ν̈́Ι	I _{OL} = .25mA
Logic "1"	_	Vcc -1.3		0.8	ν̈́Ι	I _{OL} = 1.6mA
ower		1.5	- 1	-	V	$I_{OH} = .95 mA$
		ĺ	8	13	mA	$V_{cc} = +5V$
lcc						

^{**}Typical values are at +25°C and nominal voltages.

NOTE

I. Hysteresis is defined as the amount of return required to unlatch an input. 2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.



OPERATION

The AY-5-3600 contains (see Block Diagram) a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y₀-Y₉). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still de-

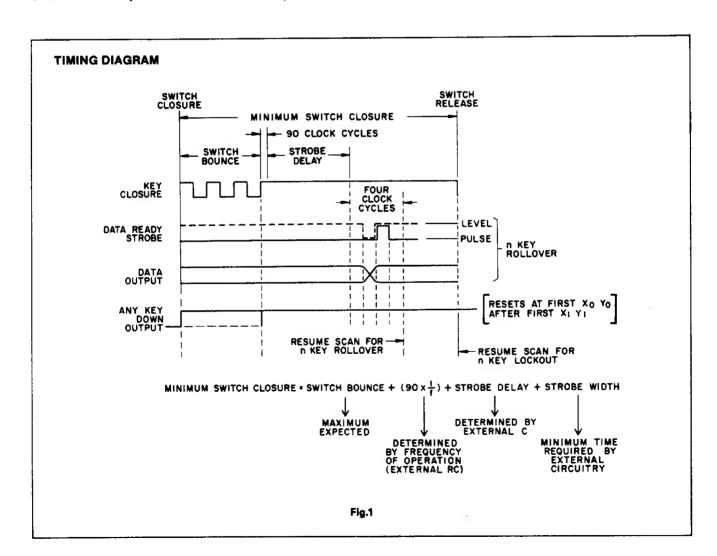
pressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).





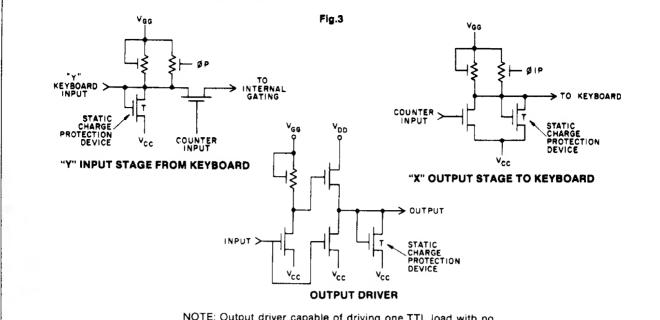
	X0 Y5	\$ X1 Y0, X0 Y8 X0 Y2 X5 Y3 X2 Y3 X2 Y2 X2 Y1 X3 Y2 X4 Y2 X0 Y5, X5 Y2 X7 Y1 X6 Y2 X7 Y2 X7 Y3 X6 Y3 X6 Y3 X8 Y1 X6 Y6 X0 Y1 X1 Y2 X4 Y2 X4 Y4 X0 Y1 X1 Y2 X4 Y3 X1 Y1 X1 Y3	X0 Y5	X1 Y2 X2 Y2 X2 Y2 X3 Y2 X4 Y2 X5 Y2 X6 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X3 Y6 X3 Y6 X3 Y6 X3 Y5 X4 Y3 X4 Y3 X4 Y3 X4 Y3 X5 Y3	SOM STX EOT END ACK BEL BS HT LF VT FF CR SO SI DLE DC:	X0 Y4 X7 Y6 X7 Y6 X3 Y7 X3 Y5 X3 Y5 X3 Y5 X1 Y7	X4 Y4 X0 Y4 X7 Y6 X3 Y7 X3 Y5 X1 Y7	C X0 Y9 X1 Y9 X4 Y4 X2 Y8 X3 Y8 X0 Y4, X8 Y9 X7 Y6 X3 Y7 X3 Y5, X1 Y6 X0 Y7, X1 Y8 X1 Y7	X5 Y0, X0' X4 Y0, X1' X4 Y2, X1' X4 Y4, X6' X4 Y1, X1' X3 Y1' X3 Y1' X3 Y1' X3 Y1' X3 Y4' X8 Y9' X3 Y7' X1 Y8' X1 Y8' X1 Y7' X1 Y7' X0 Y1' X1 Y7' X0 Y1' X0
A B C D E F G H ! J K L M N O P D R S T U V W X Y Z a b c d e ! 9		XO Y2 X5 Y3 X2 Y3 X2 Y2 X3 Y2 X3 Y2 X4 Y2 X6 Y3 X7 Y1 M6 Y2 X7 Y7 X7 Y3 X6 Y3 X6 Y3 X6 Y4 X6 Y6 X0 Y1 X1 Y2 X4 Y7 X1 Y2 X4 Y7 X4 Y7 X4 Y7 X4 Y3 X1 Y1 X1 Y3		X2 Y2 X3 Y2 X4 Y2 X5 Y2 X5 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X1 Y6 X1 Y6 X2 Y6 X2 Y6 X3 Y5 X4 Y5 X4 Y5 X6 Y1	STX ETX EOT ENG ACK BEL BS HT LF VT FF CR SO SI DLE DCI DC2 DC3 OC4	X0 Y4 X7 Y5 X3 Y7 X7 Y8 X3 Y5 X0 Y7	XO Y4 X7 Y6 X3 Y7 X3 Y5	X0 Y9 X1 Y9 X4 Y4 X2 Y8 X3 Y8 X0 Y4, X8 Y9 X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X5 Y0, X0* X4 Y0, X1* X4 Y4, X6* X4 Y1 X3 Y1 X7 Y1, X2 Y1 X3 Y4 X8 Y9 X3 Y4 X8 Y9 X1 Y8 X1 Y8 X1 Y8 X1 Y8 X1 Y7 X1 Y7 X1 Y7 X1 Y7
B C D E F G H 1 J K L M N O P D R S T U V W X Y Z a b c d e t 1 B		X5 Y3 X5 Y3 X2 Y2 X2 Y3 X4 Y2 X6 Y5, X5 Y2 X7 Y1 X6 Y2 X7 Y1 X6 Y2 X7 Y3 X8 Y1 X6 Y3 X7 Y3 X8 Y1 X6 Y3 X7 Y3 X8 Y1 X6 Y6 X7 Y1 X1 Y2 X4 Y1 X1 Y2 X4 Y1 X1 Y1 X1 Y3		X2 Y2 X3 Y2 X4 Y2 X5 Y2 X5 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X1 Y6 X1 Y6 X2 Y6 X2 Y6 X3 Y5 X4 Y5 X4 Y5 X6 Y1	STX ETX EOT ENG ACK BEL BS HT LF VT FF CR SO SI DLE DCI DC2 DC3 OC4	X0 Y4 X7 Y5 X3 Y7 X7 Y8 X3 Y5 X0 Y7	XO Y4 X7 Y6 X3 Y7 X3 Y5	X1 Y9 X4 Y4 X2 Y8 X3 Y8 X0 Y4, X8 Y9 X7 Y8 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y6	X4 Y0, X1 ' X4 Y4, X1 X4 Y4, X1 X4 Y4, X1 X3 Y1 X7 Y1, X2 Y4 X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X1 Y7 X1 Y8 X1 Y7 X1 Y8 X1 Y7 X1 Y1 X1 Y7 X1 Y1 X1 Y7
C D E F G H ! J K L M N O P G P S T U V W X Y Z Z Z Z D C C C E ! S		X2 Y3 X2 Y2 X3 Y2 X4 Y2 X6 Y3 X7 Y1 X6 Y2 X7 Y1 X6 Y2 X7 Y2 X7 Y3 X6 Y3 X8 Y1 X6 Y6 X7 Y3 X7 Y3 X7 Y4 X7 Y3 X8 Y1		X2 Y2 X3 Y2 X4 Y2 X5 Y2 X5 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X1 Y6 X1 Y6 X2 Y6 X2 Y6 X3 Y5 X4 Y5 X4 Y5 X6 Y1	ETX EOT ENG ACK BEL BS HT LF VT FF CR SO SI DLE DCT DCC2 DCC3	X0 Y4 X7 Y5 X3 Y7 X7 Y8 X3 Y5 X0 Y7	XO Y4 X7 Y6 X3 Y7 X3 Y5	X2 Y8 X3 Y8 X0 Y4, X6 Y9 X7 Y8 X3 Y7 X7 Y8, X1 Y6 X0 Y7, X1 Y8	X4 Y4, X6 Y4, X6 Y4 Y1 X3 Y1 X7 Y1, X2 Y2 X6 Y1, X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y7 X1 X1 Y7 X1
D E F G M 1 J K C M N O P O R S T U V W X Y Z a b c d d e 1 9		X2 Y3 X2 Y2 X3 Y2 X4 Y2 X6 Y3 X7 Y1 X6 Y2 X7 Y1 X6 Y2 X7 Y2 X7 Y3 X6 Y3 X8 Y1 X6 Y6 X7 Y3 X7 Y3 X7 Y4 X7 Y3 X8 Y1		X3 Y2 X4 Y2 X5 Y2 X6 Y2 X1 Y2 X0 Y5 X0 Y4 X6 Y6 X3 Y6 X2 Y6 X3 Y5 X4 Y5 X1 Y3 X1 Y3 X1 Y3 X2 Y3 X4 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3 X7 Y3	EOT ENG ACK BEL BS HT LF VT FF CR SO SU DLE DC1 DC2 DC3 DC4	X0 Y4 X7 Y5 X3 Y7 X7 Y8 X3 Y5 X0 Y7	XO Y4 X7 Y6 X3 Y7 X3 Y5	X2 Y8 X3 Y8 X0 Y4, X8 Y9 X7 Y8 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X4 Y4, X6 Y4, X6 Y4 Y1 X3 Y1 X7 Y1, X2 Y2 X6 Y1, X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y7 X1 X1 Y7 X1
DEFECH!JK LMNOPORST UVWXYZ DOCC		X Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y		X4 Y2 X5 Y2 X6 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X3 Y6 X3 Y6 X3 Y5 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X1 Y3 X2 Y3 X6 Y3 X6 Y3	ENG ACK BEL BS HT LF VT FF CR SO SI DLE DLE DC1 DC2 OC3	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	XO Y4 X7 Y6 X3 Y7 X3 Y5	X2 Y8 X3 Y8 X0 Y4, X8 Y9 X7 Y8 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X4 Y1 X3 Y1 X7 Y1, X2 Y X6 Y1, X3 Y X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X1 Y7, X1 Y
EFFGH!JKLMNOPORRSTUVWXYZ		X2 Y1 X3 Y2 X4 Y2 X6 Y5, X5 Y2 X7 Y1 W6 Y2 X7 Y2 X7 Y2 X7 Y3 X6 Y3 X8 Y1 X6 Y3 X8 Y1 X6 Y6 X0 Y1 X1 Y2 X4 Y7 X0 Y1 X1 Y2 X1 Y1 X1 Y3		X5 Y2 X6 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X2 Y6 X2 Y6 X3 Y5 X4 Y5 X1 Y3 X1 Y3 X1 Y3 X2 Y3 X4 Y3 X6 Y3	ENG ACK BEL BS HT LF VT FF CR SO SI DLE DLE DC1 DC2 OC3	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	X7 Y6 X3 Y7 X3 Y5	X3 Y8 X0 Y4, X8 Y9 X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X3 Y1 X7 Y1, X2 Y X6 Y1, X3 Y X8 Y9 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y
FGH!JKLMNOPORSTJVWKY?		X3 Y2 X7 Y1 X7 Y1 X7 Y2 X7 Y2 X7 Y2 X7 Y2 X7 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3 X7 Y3 X6 Y1 X1 Y2 X1 Y2 X2 Y4 X4 Y3 X1 Y1 X1 Y3		X6 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X2 Y6 X2 Y6 X3 Y6 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X1 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3	ACK BEL BS HT LF VT FF CR SO SI DCI DC2 OC3 OC4	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	X7 Y6 X3 Y7 X3 Y5	X3 Y8 X0 Y4, X8 Y9 X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X7 Y1, X2 Y X6 Y1, X3 Y X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y
G H		X4 Y2 X0 Y5, X5 Y2 X7 Y1 X6 Y2 X7 Y2 X7 Y3 X6 Y3 X8 Y1 X6 Y3 X8 Y1 X6 Y6 X0 Y1 X1 Y2 X4 Y1 X0 Y1 X1 Y1 X1 Y3		X6 Y2 X7 Y2 X0 Y5 X0 Y4 X6 Y6 X2 Y6 X2 Y6 X3 Y6 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X1 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y3	BEL BS HT LF VT FF CR SO SI DLE DC! OC2 OC3 OC4	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	X7 Y6 X3 Y7 X3 Y5	X3 Y8 X0 Y4, X8 Y9 X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X6 Y1, X3 Y X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y X1 Y7
H I I I I I I I I I I I I I I I I I I I		X4 Y2 X0 Y5, X5 Y2 X7 Y1 X6 Y2 X7 Y2 X7 Y3 X6 Y3 X8 Y1 X6 Y3 X8 Y1 X6 Y6 X0 Y1 X1 Y2 X4 Y1 X0 Y1 X1 Y1 X1 Y3		X7 Y2 X0 Y5 X0 Y4 X6 Y6 X3 Y6 X3 Y5 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X1 Y3 X6 Y3 X6 Y3 X6 Y3	BS HT LF VT FF CR SO SI DCI DC2 OC3 OC4	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	X7 Y6 X3 Y7 X3 Y5	X3 Y8 X0 Y4, X8 Y9 X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X6 Y1, X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y K1 Y7 X1 Y7
H		XO Y5, X5 Y2 X7 Y1 X6 Y2 X7 Y3 X6 Y6, X8 Y2 X7 Y3 X6 Y6 X6 Y6 X0 Y1 X1 Y2 X4 Y7 X0 Y1 X1 Y2 X4 Y7 X1 Y1 X1 Y3		X0 V5 X0 V4 X6 V6 X3 V6 X3 V6 X3 V5 X4 V5 X0 V2, X0 V3 X1 V3 X2 V3 X4 V3 X6 V3 X6 V3	HT LF VT FF CR SO SI DLE DC1 DC2 DC2 DC3	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	X7 Y6 X3 Y7 X3 Y5	X0 Y4, X8 Y9 X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X3 Y4 X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y
K L L M M M M M M M M M M M M M M M M M		X7 Y1 X6 Y2 X7 Y3 X6 Y3 X6 Y3 X6 Y3 X6 Y1 X6 Y6 X0 Y1 X1 Y2 X4 Y1 X0 Y1 X4 Y3 X1 Y1 X1 Y3		X0 V4 X6 V6 X3 V6 X2 V6 X3 V5 X4 V5 X0 V2, X0 V3 X1 V3 X2 V3 X6 V3 X5 V3	HT LF VT FF CR SO SI DLE DC1 DC2 DC2 DC3	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	X7 Y6 X3 Y7 X3 Y5	X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X8 Y9 X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y X1 Y7
	X2 Y6	X1 Y3 X1 Y3 X1 Y3 X1 Y3 X1 Y3 X1 Y1 X1 Y2 X2 Y4 X3 Y1 X4 Y3 X1 Y1 X1 Y3 X1 Y1 X1 Y3	X2 Y6	X6 Y6 X3 Y6 X3 Y6 X3 Y5 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X2 Y3 X2 Y3 X4 Y3 X5 Y3	LF VT FF CR SO SI DLE DCI DC2 DC3 OC3	X7 Y6 X3 Y7 X7 Y8 X3 Y5 X0 Y7	X7 Y6 X3 Y7 X3 Y5	X7 Y6 X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X3 Y7 X7 Y8 X1 Y6 X0 Y7, X1 Y X1 Y7
	X2 Y6	X7 Y2 X7 Y6, X8 Y2 X7 Y6, X8 Y1 X6 Y3 X8 Y1 X6 Y6 X0 Y1 X1 Y2 X2 Y7 X4 Y7 X0 Y1 X1 Y1 X1 Y3	X2 Y6	X6 Y6 X3 Y6 X3 Y6 X3 Y5 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X2 Y3 X2 Y3 X4 Y3 X5 Y3	VT FF CR SO SH DLE DC1 DC2 DC3 DC3	X3 Y7 X7 Y8 X3 Y5 X0 Y7	X3 Y7 X3 Y5	X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X7 Y8 X1 Y6 X0 Y7, X1 Y X1 Y7
	X2 V6	X7 Y2 X7 Y6, X8 Y2 X7 Y6, X8 Y1 X6 Y3 X8 Y1 X6 Y6 X0 Y1 X1 Y2 X2 Y7 X4 Y7 X0 Y1 X1 Y1 X1 Y3	X2 Y6	X3 Y6 X2 Y6 X3 Y5 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X2 Y3 X2 Y3 X4 Y3 X5 Y3	FF CR SO SI DLE DCI DCI DC2 DC3 DC3	X7 Y8 X3 Y5 X0 Y7	X3 Y5	X3 Y7 X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X7 Y8 X1 Y6 X0 Y7, X1 Y X1 Y7
	x2 v6	X2 Y6, X8 Y2 X7 Y3 X6 Y3 X8 Y1 X8 Y1 X6 Y6 X0 Y1 X3 Y1 X4 Y7 X4 Y7 X1 Y1 X1 Y3	X2 Y6	K2 Y6 X3 Y5 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X2 Y3 X4 Y3 X5 Y3	CR SO SI DLE DCI DC2 DC3 DC3	X3 Y5 X0 Y7	X3 Y5	X7 Y8 X3 Y5, X1 Y6 X0 Y7, X1 Y8	X7 Y8 X1 Y6 X0 Y7, X1 Y X1 Y7
	A. 10	X1 Y3 X6 Y3 X6 Y3 X6 Y4 X6 Y6 X6 Y6 X6 Y6 X6 Y6 X6 Y6 X6 Y6 X6 Y6 X6 Y6 X6 Y6 X6 Y7 X6 Y6 X6 Y7 X6 Y7 X7 X7 X7 X7 X7 X7 X7 X7 X7 X7 X7 X7 X7	X2 Y6	X3 Y5 X4 Y5 X0 Y2, X0 Y3 X1 Y3 X2 Y3 X4 Y3 X5 Y3	SO SI DLE DCI DC2 DC3 DC4	X3 Y5 X0 Y7		X3 Y5, X1 Y6 X0 Y7, X1 Y8	X1 Y6 X0 Y7, X1 Y X1 Y7
		14 A S A S A S A S A S A S A S A S A S A		X4 Y5 X0 Y2, X0 Y3 X1 Y3 X2 Y3 X4 Y3 X5 Y3	SO SI DLE DCI DC2 DC3 DC4	X0 Y7		X0 Y7, X1 Y8	X0 Y7, X1 Y X1 Y7
		X8 YI X6 Y6 X0 Y1 X3 Y1 X1 Y2 X4 Y7 X0 Y1 X4 Y3 X1 Y3		X4 Y5 X0 Y2, X0 Y3 X1 Y3 X2 Y3 X4 Y3 X5 Y3	SI DLE DCI DC2 DC3 DC4		XI Y7		X0 Y7, X1 Y X1 Y7
A STATE OF THE STA		X8 YI X6 Y6 X0 Y1 X3 Y1 X1 Y2 X4 Y7 X0 Y1 X4 Y3 X1 Y3		X0 Y2, X0 Y3 X1 Y3 X2 Y3 X4 Y3 X6 Y3	DLE DC1 DC2 DC3 DC4	X1 Y7	X1 Y7		X1 Y7
		X6 Y6 X0 Y1 X3 Y1 X1 Y2 X4 Y7 X0 Y1 X4 Y3 X1 Y1 X1 Y3		X1 Y3 X2 Y3 X4 Y3 X5 Y3	DC1 DC2 DC3 DC4		2	^' ''	
		X0 Y1 X3 Y1 X1 Y2 X4 Y4 X0 Y1 X4 Y3 X1 Y1 X1 Y3		X1 Y3 X2 Y3 X4 Y3 X5 Y3	DC1 DC2 DC3 DC4				
		X3 Y1 X1 Y2 X4 Y7 X0 Y1 X4 Y3 X1 Y1 X1 Y3		X2 Y3 X4 Y3 X5 Y3	0C2 0C3 0C4		I		, KUYI
		X3 Y1 X1 Y2 X4 Y7 X0 Y1 X4 Y3 X1 Y1 X1 Y3		X2 Y3 X4 Y3 X5 Y3	DC3 DC4			I	X5 Y1
		X Y2 X4 Y7 X0 Y1 X4 Y3 X1 Y1 X1 Y3		X4 Y3 X5 Y3	OC4		1	I	X6 Y7
		X4 Y7 X0 Y1 X4 Y3 X1 Y1 X1 Y3	ŀ	X5 Y3				1	
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	¥5 Y3		X5 Y3						X1 Y4
	X2 Y3		X2 Y3		CS		I		X7 Y6
	X2 Y2				. As	X1 Y4	X1 Y4	XI Y4	
			X2 Y2		ll us	X2 Y7	K2 Y7	X2 Y7	
	K2 Y1		X7 Y1		SP	X3 Y3, X4 Y9			X2 Y7
	X3 Y2		X3 Y2		1 3"		X4 Y9, X3 Y3	X4 Y9, X3 Y3	X4 Y9, X3 Y
1	X4 Y2		X4 Y2		N ' I	X5 Y9	X5 Y9, X0 Y9	X5 Y9	X5 Y9
İ	X5 Y2				11 -	X3 Y9	X3 Y9, X7 Y5, X1 Y9	X3 Y9	X3 Y9, X7 Y
			¥5 Y2			XB Y9	X6 Y9, X2 Y0		
	X7 Y !		X7 Y1		\$			X6 Y9.	X6 Y9
	X6 Y2		X6 Y2			X2 Y5	X2 Y5, X3 Y0	X2 Y5	X2 Y5
	X7 Y2, X2 Y9		X7 Y2			X1 YS	X1 Y5, X4 Y0	X1 Y5	X1 Y5
1	XB Y2				8	X6 Y8	X6 Y0, X6 Y8, X2 YB	X8 Y8	X6 Y8
. [X8 Y2		11 , 1	X7 Y5	X3 Y8		
	X7 Y3, X1 Y6		X7 Y3		11 / 1			X7 Y5	X7 Y4
	X6 Y3, X1 Y8		X6 Y3		11 1 1	X7 Y9	X7 Y4, X3 Y4, X8 Y0	X7 Y9	x7 Y9
- 1	X8 Y1	i	XB YI			X4 YB	X4 YB, X5 Y7, X8 Y9	X4 Y8	X4 Y8
- 1					11	X5 Y8	X5 Y8, X7 Y0, X5 Y4	X5 Y8	
1	X6 Y5, X0 Y8		X6 Y6		11 · 1	XO YE	X0 Y6, X5 Y6, X7 Y7		X5 Y8
1	XO Y I		XOYI		H		-0 10, A3 18, A/ 1/	X0 Y6	X0 Y6, X7 Y
1	X3 Y1		X3 Y1		11	X8 Y3	X8 Y3	X8 Y3	X8 Y3
1	X1 Y2				n — 1	X2 Y4	X2 Y4, X8 Y7	X2 Y4	X8 Y7
Ī			X3 Y2		11	X8 Y4	XB Y4	X8 Y4	
	X4 Y1		X4 Y1		1 1	X7 Y4	""		X8 Y4
	X6 Y1		X6 Y1		14 '		1	X7 Y4	
ı	X4 Y3		X4 Y3		0	X6 Y7, X8 Y8	XB Y8	X6 Y7, X8 Y8	X8 Y8
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1	XS Y1	l	X5 Y1			X2 Y6	1	X2 Y0	
1	X0 Y3		X0 Y3		•	X3 Y0	1	X3 Y0	
1		i	AU TJ		5	X4 Y0	į l	X4 Y0	
- 1	ı	X8 Y6, X2 Y9	1	X4 Y6, X8 Y6	6	X5 YO, X2 Y8	į į		
- 1	ŀ			XI YI	;		[[X5 Y0	
ł	X8 Y6	X1 Y6	X8 Y6			X6 YO, X3 YB	1	X0 Y0	
- 1			A0 10	XB Y1	0	X7 Y0	1 1	X7 YO	
- 1		X1 YB	Į.	X2 Y4	9	X6 Y0, X8 Y9	1	X8 Y0	
- 1	X4 Y7, X8 Y7		X4 Y7, X8 Y7	X4 Y7	11 1	X5 Y4	ا سمسا		
- 1	X3 Y6	X3 Y6	X3 Y6		ii l		X8 Y5	X5 Y4	XB Y5
4	X4 Y5				IJ - L	X8 Y5, X5 Y8	1	X8 Y5, X5 Y6	
1	,•	X4 Y5	X4 Y5			X6 Y5	X7 Y8, X6 Y5, X0 Y0	X6 Y5	
	1	1		X6 Y4	11 - 1	X6 Y4, X7 Y7			
L	1	I	X2 YS	X2 Y9			X7 Y7, X6 Y4, X4 Y7	X6 Y4	
ונו ו	X5 Y7	X5 Y7	X5 Y7, X0 Y8			X5 Y5	X5 Y5, X5 Y0, X0 Y7	X5 Y5	
	- · · · I	~~·· [AS T/, AU TB	X5 Y7, X0 Y8	}	X4 Y6	X4 Y6, X7 Y4	X4 Y6	
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71 0 1. Bi		of the AY-5-3600 c	prrespond to bire 1	to 7 of ASC II					

Fig.2 STANDARD AY-5-3600 CODE ASSIGNMENTS ASCINCODE

OPTIONS PROVIDED WITH STANDARD ENCODER

- Device Marking: AY-5-3600
- Internal Oscillator on Pin Nos. 1, 2, 3
- Any Key Output on Pin No. 4
- Any Key Output True (Logic 1) During Key Depression
- Output Data Bit B10 on Pin No. 5

- N-Key Rollover Only
- True Outputs Only
- Pulse Data Ready Signal
- Internal Resistor to V_{DD} on Shift/Control Pin
- Plastic Package



NOTE: Output driver capable of driving one TTL load with no external resistor. Capable of driving two TTL loads using an external 6.8K Ω resistor to $V_{\rm tot}$.

TYPICAL CHARACTERISTIC CURVES

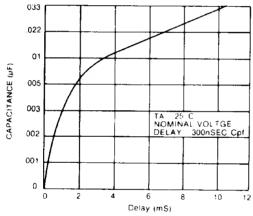


Fig.4 STROBE DELAY vs. C.

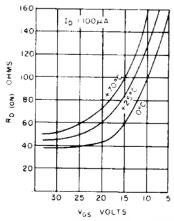


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

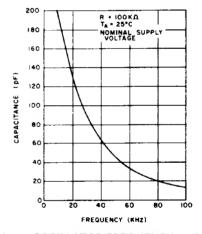


Fig.5 OSCILLATOR FREQUENCY vs. C₂

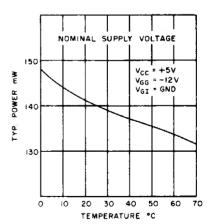


Fig.7 TYPICAL POWER CONSUMPTION (mW)